

CLAIMS:

1. A transistor-type ferroelectric nonvolatile memory element having an MFMIS (metal-ferroelectric-metal-insulator-semiconductor) structure, comprising:

an MFM (metal-ferroelectric-metal) structure and an MIS (metal-insulator-semiconductor) structure stacked up and down; and

means for increasing the effective area of a capacitance of the lower MIS structure as compared with the effective area of a capacitance of the upper MFM structure.

2. A transistor-type ferroelectric nonvolatile memory element according to claim 1, further having a semiconductor substrate and a trench formed in the semiconductor substrate, wherein the MIS structure is formed in the trench, the MFM structure is laminated on the trench nearly in parallel with the main surface of the semiconductor substrate, and means for increasing the effective area is the trench.

3. A transistor-type ferroelectric nonvolatile memory element according to claim 2, wherein the MIS structure is an MIS transistor of the nonvolatile memory element, the regions of source, base and drain of the MIS transistor are formed in the semiconductor substrate in order of source, base and drain

from the lower side, and means for increasing the effective area is a gate structure of the MIS transistor formed on the inner surface of the trench.

4. A transistor-type ferroelectric nonvolatile memory element according to claim 2, wherein the MIS structure is an MIS transistor of the nonvolatile memory element, the regions of source, base and drain of the MIS transistor are formed in the semiconductor substrate in order of drain, base and source from the lower side, and means for increasing the effective area is a gate structure of the MIS transistor formed on the inner surface of the trench.

5. A transistor-type ferroelectric nonvolatile memory element according to claim 2, wherein the MIS structure is a MIS transistor of the nonvolatile memory element, and the regions of source and drain of the MIS transistor are isolated by the trench.

6. A transistor-type ferroelectric nonvolatile memory element according to claim 1, wherein the MIS structure includes a rugged portion therein, means for increasing the effective area is constituted by the rugged portion, the upper part of the MIS structure is flat, and the MFM structure is laminated thereon.

7. A transistor-type ferroelectric nonvolatile memory element according to claim 1, wherein means for increasing the effective area is constituted by an MIM (metal-insulator-metal) structure provided between the MFM structure and the MIS structure.

8. A transistor-type ferroelectric nonvolatile memory element according to claims 2 to 7, wherein the effective area of a metal layer on the ferroelectric layer of the MFM structure is smaller than that of the ferroelectric layer.